Code No: **19ECT503**

R19

III B. TECH I SEMESTER REGULAR EXAMINATIONS, FEB - 2022
VLSI DESIGN
(Electronics And Communication Engineering)

Time: 3 Hours **Max. Marks: 60**

Note: Answer **ONE** question from each unit **(5 × 12 = 60 Marks)**

~~~~~~

UNIT-I

1. a) Explain in detail about the flow diagram of the Berkeley CMOS n-well fabrication. [7M]

   b) Compare and contrast CMOS technology and Bipolar technology. [5M]

(OR)

2. a) Explain about the λ-based CMOS Design rules and discuss with a layout example. [4M]

   b) In the inverter circuit, what is meant by pull up and pull down? Derive the required ratio between the pullup and pull-down transistor sizes, if an nMOS inverter is to be driven from another nMOS inverter. [8M]

UNIT-II

3. a) Derive the expression for the rise time delay of a CMOS inverter. [6M]

   b) What is wiring capacitance? Explain in detail about the three sources of wiring capacitance. [6M]

(OR)

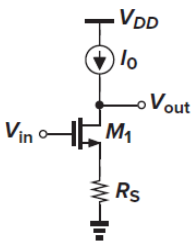
4. a) Compare and contrast the constant electric field scaling and constant voltage scaling with two examples. [6M]

   b) Discuss about the limitations of scaling. [6M]

UNIT-III

5. a) Define the following terms (i) Body bias effect (ii) Channel length modulation. [6M]

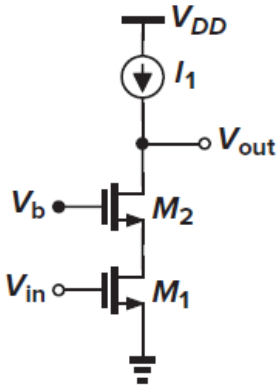
   b) Calculte the voltage gain for the following circuit. (Assume I0 is ideal current source) [6M]


~~~~~~

(OR)

6. a) Differentiate the common source and common drain amplifier. [4M]

   b) Calculate the voltage gain of the following circuit. [8M]



UNIT-IV

7. a) Explain pass transistor logic. Design a 2:1 MUX using pass transistor logic. [6M]

   b) How a large fan-in of a circuit affects the delay. What is its remedy. [6M]

(OR)

8. a) What is charge leakage? Explain how a static bleeder helps to resolve the issue of charge leakage. [6M]

   b) Design a master slave edge triggered D flip flop using the transmission gates. And explain its operation. [6M]

UNIT-V

9. a) Write about FPGA Programming Technologies in detail. [6M]

   b) Write about Programmable I/O blocks in FPGAs. [6M]

(OR)

10. a) Draw the design flow of field programmable gate arrays and discuss about its routing architecture. [6M]

    b) Explain in detail about the architecture of Xilinx cool runner. [6M]

* * * * *